IN THE CLAIMS

1. (Currently Amended) A low-pass filter with a variable gain, comprising:

a transconductance differential amplifier stage mounted in an open loop including

a first differential input and a second differential input, and

a first differential output and a second differential output,

with the first differential input and the second differential input having a given frequency range;

a passive circuit connected between~~to~~ the first differential output and the second differential output, the passive circuit for providing low-pass filtering of the differential amplifier stage whose cut-off frequency is below the frequency range to be amplified; and

a control element for controlling a bias point of the differential amplifier stage so as to regulate a gain thereof.

2. (Original) The low-pass filter according to claim 1, wherein the differential amplifier stage further comprises:

a first transistor with a source, a gate, and a drain, wherein the gate of the first transistor receives a first portion of the differential input to be filtered;

a second transistor with a source, a gate, and a drain, wherein the gate of the second transistor receives a second portion of the differential input to be filtered;

a third transistor and a fourth transistor each with a source, a drain and a gate configured for setting the bias point of differential amplifier stage;

a fifth transistor with a source, a drain and a gate, and constituting a power source for the first transistor and the second transistor; and

wherein a bias current of the third transistor, the fourth transistor and the fifth transistor are controlled by the control element.

3. (Original) The low-pass filter according to claim 2, wherein the passive circuit for providing the low-pass filtering is a first-order filter realized by at least one capacitive

element and an intrinsic drain-source resistance of one or more of the first transistor, the second transistor, the third transistor, and the fourth transistor.

4. (Original) The low-pass filter according to claim 3, further comprising:

a resistor connected between the drain of the first transistor and the drain of the second transistor.

5. (Original) The low-pass filter according to claim 4, wherein the capacitive element is one or more MOS-type transistor.

6. (Original) The low-pass filter according to claim 2, wherein the source of the first transistor and the source of the second transistor are connected to the drain of the fifth transistor;

wherein the source of the fifth transistor is connected to a first reference voltage;

wherein the drain of the first transistor is connected to the drain of the third transistor and the source of the third transistor is connected to a second reference voltage;

wherein the drain of the second transistor is connected to the drain of the fourth transistor and the source of the fourth transistor is connected to the second reference voltage; and

wherein the gate of the third transistor, the fourth transistor, and the fifth transistor are controlled by the control element.

7. (Original) The low-pass filter according to claim 6, wherein the control element comprises:

a sixth transistor with a source, a drain and a gate, the source of the sixth transistor connected to the second reference voltage, and the drain of the sixth transistor receiving a control voltage;

a seventh transistor with a source, a drain and a gate, the source of the seventh transistor connected to the second reference voltage, and the gate of the seventh transistor being connected to the gate of the sixth transistor, the third transistor, and the fourth transistor, and to the control voltage;

a eighth transistor with a source, a drain and a gate, the source of the eighth transistor connected to the first reference voltage, and the drain and the gate of the eighth transistor both connected to the drain of the seventh transistor and to the gate of the fifth transistor.

8. (Original) The low-pass filter according to claim 1, wherein the first transistor, the second transistor, and the fifth transistor are NMOS-type and wherein the third transistor and the fourth transistor are PMOS-type.

9. (Original) The low-pass filter according to claim 2, wherein the first transistor, the second transistor, and the fifth transistor are NMOS-type and wherein the third transistor and the fourth transistor are PMOS-type.

10. (Original) The low-pass filter according to claim 4, wherein the first transistor, the second transistor, and the fifth transistor are NMOS-type and wherein the third transistor and the fourth transistor are PMOS-type.

11. (Original) The low-pass filter according to claim 6, wherein the first transistor, the second transistor, and the fifth transistor are NMOS-type and wherein the third transistor and the fourth transistor are PMOS-type.

12. (Original) The low-pass filter according to claim 7, wherein the first transistor, the second transistor, and the fifth transistor are NMOS-type and wherein the third transistor and the fourth transistor are PMOS-type.

13. (Currently Amended) A semiconductor product for frequency reception tuning, the semiconductor product comprising:

a transconductance differential amplifier stage mounted in an open loop including

a first differential input and a second differential input, and

a first differential output and a second differential output,

with the first differential input and the second differential input having a given frequency range;

a low-pass filter for providing low-pass filtering of the differential amplifier stage, the low-pass filter with a cut-off frequency below the frequency range to be amplified, the low-pass filter including a passive circuit connected between~~to~~ the first differential output and the second differential output; and

a control element for controlling a bias point of the differential amplifier stage so as to regulate a gain thereof.

14. (Original) The semiconductor product according to claim 13, wherein the differential amplifier stage further comprises:

a first transistor with a source, a gate, and a drain, wherein the gate of the first transistor receives a first portion of the differential input to be filtered;

a second transistor with a source, a gate, and a drain, wherein the gate of the second transistor receives a second portion of the differential input to be filtered;

a third transistor and a fourth transistor each with a source, a drain and a gate configured for setting the bias point of differential amplifier stage;

a fifth transistor with a source, a drain and a gate, and constituting a power source for the first transistor and the second transistor; and

wherein a bias current of the third transistor, the fourth transistor and the fifth transistor are controlled by the control element.

15. (Original) The semiconductor product according to claim 14, wherein the passive circuit for providing the low-pass filtering is a first-order filter realized by at least one capacitive element and an intrinsic drain-source resistance of one or more of the first transistor, the second transistor, the third transistor, and the fourth transistor.

16. (Original) The semiconductor product according to claim 15, further comprising:

a resistor connected between the drain of the first transistor and the drain of the second transistor.

17. (Original) The semiconductor product according to claim 16, wherein the capacitive element is one or more MOS-type transistors.

18. (Original) The semiconductor product according to claim 14, wherein the source of the first transistor and the source of the second transistor are connected to the drain of the fifth transistor;

wherein the source of the fifth transistor is connected to a first reference voltage;

wherein the drain of the first transistor is connected to the drain of the third transistor and the source of the third transistor is connected to a second reference voltage;

wherein the drain of the second transistor is connected to the drain of the fourth transistor and the source of the fourth transistor is connected to the second reference voltage; and

wherein the gate of the third transistor, the fourth transistor, and the fifth transistor are controlled by the control element.

19. (Original) A semiconductor product comprising:

a first transistor with a source, a gate, and a drain, wherein the gate of the first transistor receives a first portion of a differential signal to be filtered and amplified;

a second transistor with a source, a gate, and a drain, wherein the gate of the second transistor receives a second portion of the differential signal;

a third transistor and a fourth transistor each with a source, a drain and a gate configured for setting a bias point of the first transistor and the second transistor;

a fifth transistor with a source, a drain and a gate, and constituting a power source for the first transistor and the second transistor;

a low-pass filter for providing low-pass filtering of the first transistor and the second transistor, the low-pass filter with a cut-off frequency below the frequency range

to be amplified, the low-pass filter including a passive circuit connected to the differential output; and

a control element for controlling the bias point of the first transistor and the second transistor so as to regulate a gain thereof;

wherein the first transistor, the second transistor, the third transistor and the fourth transistor form a differential amplifier stage;

wherein a bias current of the third transistor, the fourth transistor and the fifth transistor are controlled by the control element.

20. (Original) The semiconductor product of according to claim 19, wherein the source of the first transistor and the source of the second transistor are connected to the drain of the fifth transistor;

wherein the source of the fifth transistor is connected to a first reference voltage;

wherein the drain of the first transistor is connected to the drain of the third transistor and the source of the third transistor is connected to a second reference voltage;

wherein the drain of the second transistor is connected to the drain of the fourth transistor and the source of the fourth transistor is connected to the second reference voltage; and

wherein the gate of the third transistor, the fourth transistor, and the fifth transistor are controlled by the control element.